

REMARKS

Applicants have received the Office Action dated January 28, 2008, in which the Examiner: 1) reopened prosecution; 2) acknowledged that claims are statutory; and 3) rejected claims 1-25 under 35 U.S.C. §103(a) as allegedly obvious in view of Hunter et al. (US Pat. No. 6,194,940, hereinafter 'Hunter') and Clark et al. (US Pat. No. 6,519,707, hereinafter 'Clark').

With this Response, Applicants amend claims 1, 9, 15, 21 and 24, and cancel claims 7, 12 and 18. Applicants believe the pending claims are allowable over the art of record and respectfully request reconsideration.

I. 35 U.S.C. §101

In the Office Action dated January 28, 2008, the Office Action states "Applicant has not attempted to redefine a system, wait unit, or processor to encompass embodiments which are not within the statutory classes of invention." Applicants appreciate the Office Action acknowledging that the claims are statutory. However, if Applicants have misunderstood the preceding, Applicants would appreciate further clarification in the next Office Action.

II. REJECTIONS UNDER 35 U.S.C. §103(A)

A. Claim 1

Claim 1 was rejected as allegedly obvious over Hunter in view of Clark. Applicants amend claim 1 to more clearly define over Clark's teaching of placing the processor in sleep mode by executing instruction stored in a memory.

Hunter is directed to automatic clock switching. (Hunter Title). In particular, Hunter teaches a processor and a clock switch controller, which in response to a clock select signal from the processor or a clock interrupt signal switches to the appropriate clock. (Hunter Col. 3, lines 11-14). Hunter also teaches switching to slower clocks when a phone is in 'sleep' mode, and switching to faster clocks when the phone is in 'wake' mode. (Hunter Col. 1, lines 24-35). Thus, Hunter teaches switching clocks in response to the mode of the phone.

Clark is directed to method and apparatus for dynamic power control of a low power processor. (Clark Title). In particular, Clark teaches a processor, a voltage

regulator, and a memory. (Clark Col. 4, lines 45-47). Clark teaches that the processor executes instructions stored in memory to place the processor in sleep mode before adjusting the operating voltage of the processor by the voltage regulator. (Clark Col. 5, lines 63-67). The processor reads or writes to selected memory address locations which results in the operating voltage of the processor being changed by voltage regulator. (Clark Col. 5, lines 6-25). Thus, Clark teaches regulating the voltage of the processor by executing instructions in the memory.

Claim 1, by contrast, specifically recites “a second processor coupled to said first processor;... and said wait unit de-asserts the wait signal upon detection of a signal from said second processor.” Applicants respectfully submit that Hunter and Clark do not teach or fairly suggest such a system. Hunter teaches switching clocks in response to the mode of the phone, and Clark teaches regulating the voltage of the processor by executing instructions stored in the memory. Thus, Applicants submit that Hunter and Clark do not teach or fairly suggest “**a second processor coupled to said first processor;... and said wait unit de-asserts the wait signal upon detection of a signal from said second processor.**”

Based at least on the foregoing Applicant submits that claim 1 all claims which depend on claim 1 (claims 2-6 and 8) should be allowed.

B. Claim 9

Claim 9 was rejected as allegedly obvious over Hunter in view of Clark. Applicants amend claim 9 to more clearly define over Clark’s teaching of placing the processor in sleep mode by executing instruction stored in a memory.

Claim 9 specifically recites “causing said wait signal to de-assert upon receiving a signal from another processor, said de-assert controlled by logic external to said processor.” Applicants respectfully submit that Hunter and Clark do not teach or fairly suggest such a system. Hunter teaches switching clocks in response to the mode of the phone, and Clark teaches regulating the voltage of the processor by executing instructions stored in the memory. Thus, Applicants submit that Hunter and Clark do not teach or fairly suggest “**causing said wait signal to de-assert upon receiving a signal from another processor**, said de-assert controlled by logic external to said processor.”

Based at least on the foregoing Applicant submits that claim 9 all claims which depend on claim 9 (claims 10-11 and 13-14) should be allowed.

C. Claim 15

Claim 15 was rejected as allegedly obvious over Hunter in view of Clark. Applicants amend claim 15 to more clearly define over Clark's teaching of placing the processor in sleep mode by executing instruction stored in a memory.

Claim 15 specifically recites "a second processor interface;... and said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface." Applicants respectfully submit that Hunter and Clark do not teach or fairly suggest such a system. Hunter teaches switching clocks in response to the mode of the phone, and Clark teaches regulating the voltage of the processor by executing instructions stored in the memory. Thus, Applicants submit that Hunter and Clark do not teach or fairly suggest **"a second processor interface;... and said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface."**

Based at least on the foregoing Applicant submits that claim 15 all claims which depend on claim 15 (claims 16-17 and 19-20) should be allowed.

D. Claim 21

Claim 21 was rejected as allegedly obvious over Hunter in view of Clark. Applicants amend claim 21 to more clearly define over Clark's teaching of placing the processor in sleep mode by executing instruction stored in a memory.

Claim 21 specifically recites "a second processor;... and means for releasing said first processor from the wait state by a wait release signal from said second processor." Applicants respectfully submit that Hunter and Clark do not teach or fairly suggest such a system. Hunter teaches switching clocks in response to the mode of the phone, and Clark teaches regulating the voltage of the processor by executing instructions stored in the memory. Thus, Applicants submit that Hunter and Clark do not teach or fairly suggest **"a**

second processor;... and means for releasing said first processor from the wait state by a wait release signal from said second processor.”

Based at least on the foregoing Applicant submits that claim 21 all claims which depend on claim 21 (claims 22-25) should be allowed. Further, Applicants amend claim 24 to correspond with the amendment of claim 21.

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Incorporated's Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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